ASIP LAB Up-gradation Meeting 07.12.2017

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| **ASIPmeister** | |
| * Uses simple DLX processor with 4 pipeline delay and branch delay slots * Separate CoSy Compiler * Had bugs in .des file and GUI crash problems * Many scripts required to fix the problems * NOPs required for ModelSim/FPGA * SINAS used for new instructions * No interrupts | * Uses Brownie-32 (RISC) with full forwarding and zero branch delay slot * Integrated GCC Compiler support * No such issues * No more scripts required * No NOP * instruction are available in the generated compiler * Reset/External/Internal Interrupts |
| **DLXSim** | |
| * Uses DLX instructions and formats * Pipeline delay settings | * All the Brownie-32 instructions and Formats are implemented * Some directives are also implemented * Full-forwarding is also implemented (-pf1)   **To-do**   * Support for External/Internal Interrupts * Support for other GCC generated directives |
| **ModelSim/ISE/ISIM** | |
|  | * Whole framework is updated according to Browine-32 interface signals * Framework can be simulated in ISIM (except LCD) * Scripts to generate .mem/.coe/.mif files   **To-do**   * Support for External/Internal Interrupts * Add some debug printing in the testbench * Move to Vivado |
| **FPGA Board** | |
| * LCD was not working, and UART was not functional while using u\_print() in C application * Many NOPs required | * LCD and UART are working. No SINAS are required. * UART: Tested with bubble-sort and adpcm array printing * LCD: tested with simple text   **To-do (Virtex-5)**   * LCD Touch, and graphics to be tested * Small board for LCD, UART, Switch etc. * Need a dual supply (3.3V, 5V)   **To-do (Virtex-7)**   * Convert whole framework to Virtex-7 board * Small PCB with FMC Connector |
| **Computer Used** | |
| I80labpcXX | * New ASIPmeister is installed on i80pc57 (CentOS) * License is installed on i80asip (CentOS VM)   **To-do**   * Setting up more PC for the students |
| **Making it more attractive** | |
| **To-do**   * Change the description and title of the LAB attractive * Add pictures of FPGA board, LCD etc. * Add new applications like VGA, Bluetooth * Integrate new topics, like Hardware Security??? | 1. Customized Embedded Processor Design 2. Customized and Secure Processor Design    * 1st part: designing custom ASIPs    * 2nd Part: Investigating processor security: Trojan Insertion, Detection etc. in the processor in VHDL |